

LOW VOLTAGE ELECTRON BEAM LITHOGRAPHY

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The contract has three parts covering aspects of high precision electron beam lithography. (1) Comprehensive computer modelling of the electron beam tool. (2) Experimental determination of the properties of sources, columns, and targets, and (3) The use of silicon single crystals as straightness and orthogonality standards using orientation dependent etching techniques.

Tasks 1-4. Comprehensive modelling of the electron beam tool.

A copy of the Munro electron optical programs has been loaded onto a Sun workstation.

A comprehensive data set of Mott differential cross sections from 0.1 to 20keV across the periodic table has been loaded on to a workstation for analysis with Mathematica. The aim of using Mathematica is to determine the trends across the three dimensional surface formed by the scattering angle, the energy, and the atomic number. The goal is to find an empirical form for the Mott cross sections that can be implemented in the Monte-Carlo electron scattering programs developed under a previous contract. This is particularly important for low voltage electron beams where the screened Rutherford cross section is inaccurate.

Tasks 5-8. Experimental determination of the properties of sources, columns, and targets.

For low voltage electron beam lithography it is advantageous to scale the energy spread of the electron beam down with the energy to reduce the effects of chromatic aberrations on focus and deflection systems. Photoemissive cathodes are one type of electron source that can give stable low energy spread electron emission (1). Energy distributions of 90meV full-width at half maximum have been reported for negative affinity GaAs sources at 300K with currents up to 7 μ A and photocathodes have been demonstrated to be capable of producing up to 250 μ A of continuous current for up to 10hr with little loss in intensity. During the last reporting period we began a project to investigate the properties of highly doped GaAs photoemitters. During this period we have obtained a GaAs wafer sample and a Cs channel source.

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Task 9: Distortion and Large Feature Metrology Standard.

The aim of this work is to develop a suitable process for reliably producing silicon calibration structures in the form of orthogonal edges in four-inch diameter silicon wafers based on orientation-dependent etching procedures.

In the last reporting period we demonstrated that a very thin (20nm) silicon nitride mask was sufficient to protect silicon against a 45% KOH etch at 80C for 280 minutes. The pattern that was etched into the silicon during this etching experiment was a fan pattern of 10micron wide lines 10cm long at 0.01° intervals over $\pm 1^\circ$. Any misalignment of the wafer flat to the crystal axis (alignment spec. 0.5°) could therefore be compensated for and one line of the fan should be aligned to 0.005° . The line with the best alignment to the crystal axis could then be used to align the silicon standard pattern in a subsequent exposure and etch. The problem was to identify the line that was most closely aligned. From SEM measurements it became clear that the most closely aligned features were those that had etched least. Figure 1a shows a plot of the line width after etching for 280 minutes for the first 130 lines of the fan. It can be seen that there is a distinct minimum around line 70. However, there was insufficient etching to differentiate between the lines 65 to 71. The wafer was therefore etched for a further 8 hours for a total of 1240 minutes. There was then a more significant dip over the range 65 to 71 with a minimum at line 68. This observation gives us a method for aligning a second layer pattern to 0.005° . However an alignment to 0.005° still leaves a residual 10microns that must be etched out to force the line into perfect alignment.

A prototype pattern for the Si standard has been designed and laid out. The pattern contains a central line for alignment to the etched fan which will be used as a first level etch. The metrology pattern consists of three lines forming three sides of a 7cm square. The three lines are each triple 10micron lines at 30micron spacing. Within the square are broken lines and crosses.

A wafer holder which is of the same dimensions as a 5" mask blank has been designed to allow a MEBES IV to use a 4" wafer, figure 2.

Anticipated Work in the next reporting period.

The Munro programs will be used to model the electron optical properties of some low energy columns.

Mott differential electron scattering cross sections in tabular form will be reduced to a semi-empirical form.

A start will be made on setting up an experiment to measure the electron energy distribution from a GaAs photoelectric cathode.

The Si-standard pattern will be defined on a CAD package.

Refs.

1. C.S. Feigerie, D.T. Pierce, A. Sieler and R.J. Celotta "Intense source of monochromatic electrons: Photoemission from GaAs" Appl. Phys. Lett 44 p866 (1984)

Figure 1.

Variation of line width after a KOH anisotropic etch. The lines numbered from 0 to 200 are spaced at 0.01 degree intervals. After 280 minutes etch the alignment of the wafer around the crystalline axis shows up as a minimum in the etch rate.

Figure 2.

The schematic of the wafer holder for a MEBES machine.

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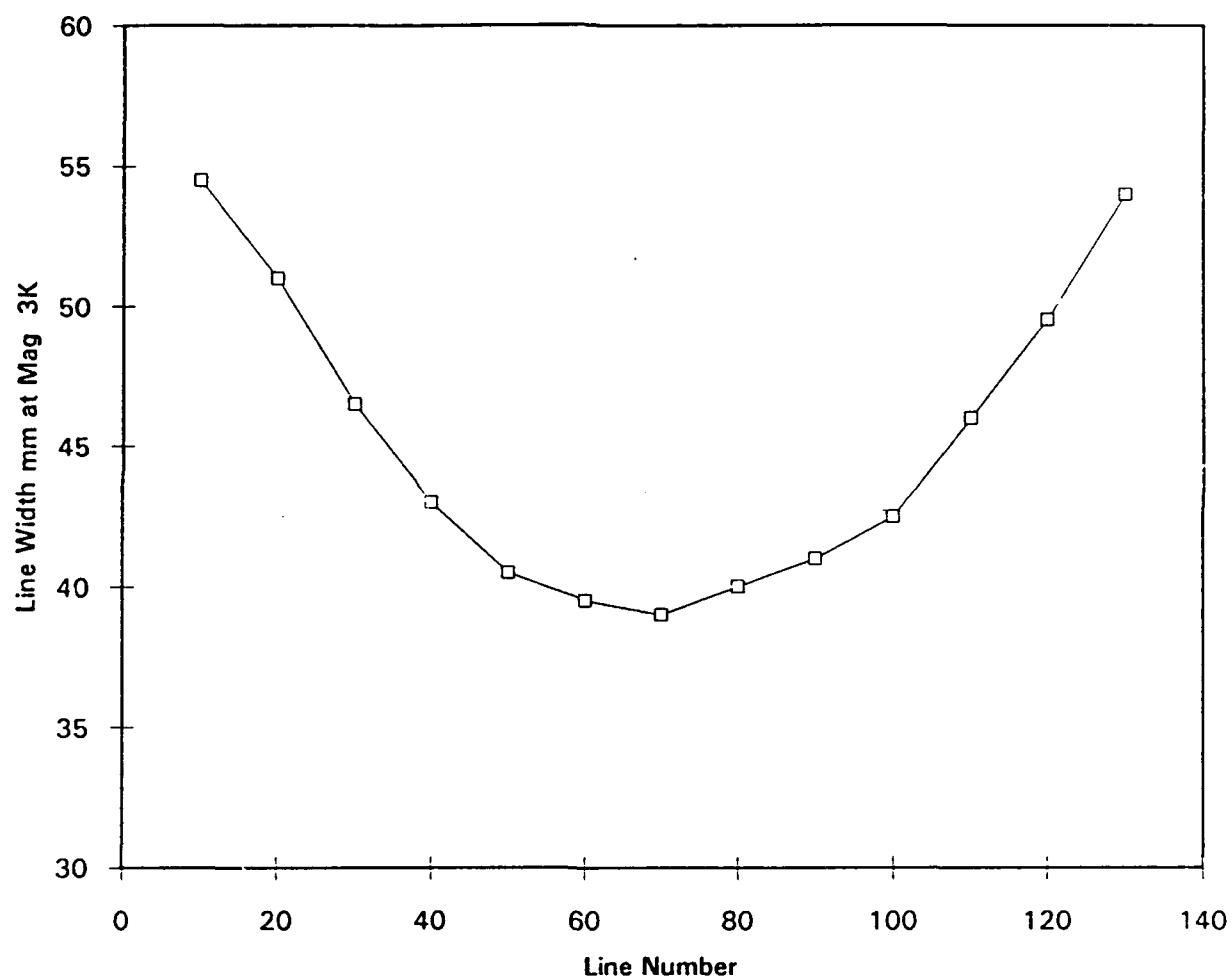
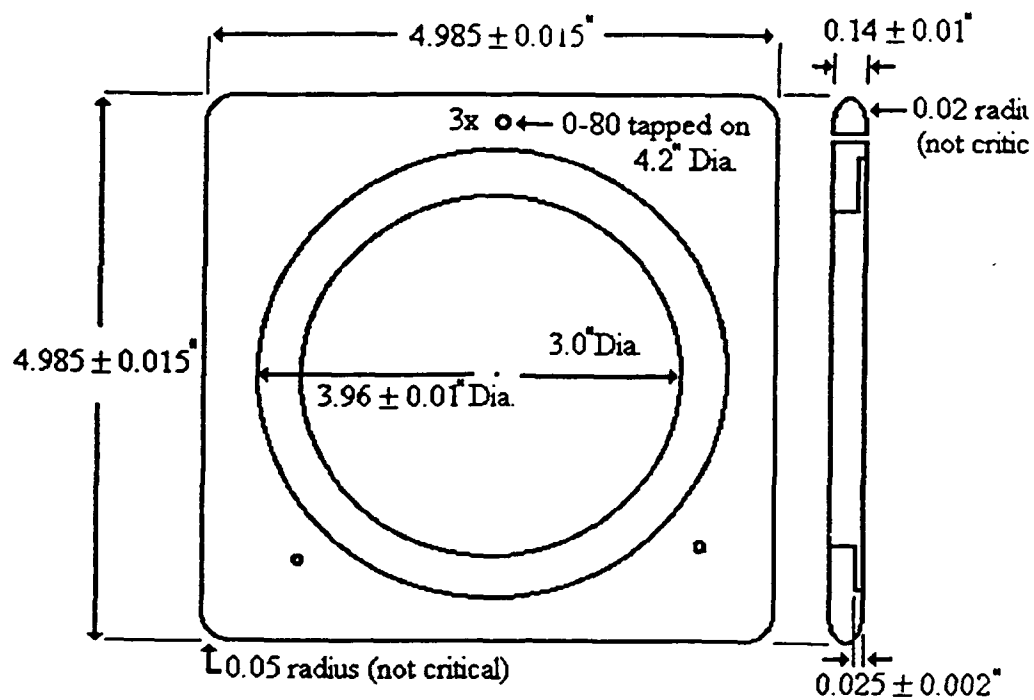


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Not to scale

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Figure 2.

The schematic of the wafer holder for a MEBES machine.